Notice of Allowability	Application No.	Applicant(s)	
	10/035,835	YUN ET AL	
	Examiner	Art Unit	
	Lina Yang	2665	
The MAILING DATE of this communication appe All claims being allowable, PROSECUTION ON THE MERITS IS herewith (or previously mailed), a Notice of Allowance (PTOL-85) NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RI of the Office or upon petition by the applicant. See 37 CFR 1.313	(OR REMAINS) CLOSED in this app or other appropriate communication GHTS. This application is subject to	olication. If not included will be mailed in due course	THIS initiative
1. This communication is responsive to 10/18/2005.		11	
2. The allowed claim(s) is/are 20,22-25,28-35,43,54,56,58-62	and 65-73.	Alfam v.	200
 3. Acknowledgment is made of a claim for foreign priority una) All b) Some* c) None of the: 1. Certified copies of the priority documents have 2. Certified copies of the priority documents have 3. Copies of the certified copies of the priority documents have International Bureau (PCT Rule 17.2(a)). * Certified copies not received: Applicant has THREE MONTHS FROM THE "MAILING DATE" onoted below. Failure to timely comply will result in ABANDONMITHIS THREE-MONTH PERIOD IS NOT EXTENDABLE. 4. A SUBSTITUTE OATH OR DECLARATION must be submit INFORMAL PATENT APPLICATION (PTO-152) which give 5. CORRECTED DRAWINGS (as "replacement sheets") must (a) including changes required by the Notice of Draftsperson (b) hereto or 2) to Paper No./Mail Date (b) including changes required by the attached Examiner's Paper No./Mail Date Identifying indicia such as the application number (see 37 CFR 1.6 each sheet. Replacement sheet(s) should be labeled as such in the following comment regarding REQUIREMENT Faces. 	been received. been received in Application No cuments have been received in this not of this communication to file a reply of ENT of this application. Ited. Note the attached EXAMINER'S is reason(s) why the oath or declaration to be submitted. The submitted on's Patent Drawing Review (PTO-9) Amendment / Comment or in the Off the submitted of the subm	eational stage application from the somplying with the requirement of the front (not the back) of the submitted. Note the submitted.	iER In the Ints OF
Attachment(s) 1. ☐ Notice of References Cited (PTO-892) 2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948) 3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08 Paper No./Mail Date 4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material	5. ☐ Notice of Informal Pa 6. ☑ Interview Summary (I Paper No./Mail Date 7. ☑ Examiner's Amendmen 8. ☑ Examiner's Statemen 9. ☐ Other	PTO-413), ent/Comment	

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DETAILED ACTION

1. This communication is in response to applicant's 10/06/2005 Amendment.

Claims 1-19, 21, 26-27, 36-42, 44-53, 55, 57, 63-64 have been cancelled. Claims independent claims 20, 25, 43, 54, 62 have been amended. New claims 72-73 have been added. Claims 20, 22-25, 28-35, 43, 54, 56, 58-62, 65-73 are pending.

Examiner's Amendment

2. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Gerald Maliszewski on 12/19/2005.

The claims have been amended by the examiner as the following.

Claim 20 (page2 line 18), "the crossbar selected from the crossbar counter list" has been replaced by "a crossbar selected from the crossbar counter list".

Claim 43 (page 8 line 17), "information packets across the links[.]" has been replaced by "information packets across the links [:] and".

Allowable Subject Matter

3. Claims 20, 22-25, 28-35, 43, 54, 56, 58-62, 65-73 are allowed.

The following is an examiner's statement of reasons for allowance.

The subject matter of claims 20, 22-24 is allowable over prior art of record, because all prior arts fail to teach or suggest a hierarchical arbitration method for a switch system including a first plurality of crossbars with a plurality of parallel routed switch inputs and a plurality of parallel routed switch outputs, comprising:

establishing a crossbar counter list;

accepting variably sized information packets including a plurality of cells, at a plurality of switch inputs, the plurality of information packets addressing a plurality of switch outputs;

simultaneously arbitrating for a plurality of links between switch inputs and switch outputs in a plurality of arbitration cycles for each crossbar, where each switch output in a crossbar simultaneously nominates an available switch input:

locking the links;

transferring information packets across the links; and,

wherein simultaneously arbitrating for a plurality of links between switch inputs and switch outputs, for each of the first plurality of crossbars, includes arbitrating between a plurality of available switch inputs, in response to the crossbar selected from the crossbar counter list, as recited in the claims

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The subject matter of claims 25, 28–35 is allowable over prior art of record, because all prior arts fail to teach or suggest a hierarchical arbitration method in a switch system including a first plurality of crossbars with a plurality of parallel routed switch inputs and a plurality of parallel routed switch outputs, comprising:

accepting variably sized information packets including a plurality of cells at a plurality of switch inputs, the plurality of information packets addressing a plurality of switch outputs;

at each switch input, queuing the information packets into a plurality of queues; simultaneously arbitrating for a plurality links between switch inputs and switch outputs;

locking the links:

selecting a queue for each locked link, for each crossbar, by selecting the least recently available queue as follows:.

for each switch input, establishing a queue list with a queue pointer; at a first crossbar, selecting a first queue for each switch input accepting a nominating switch output, in response to the queue pointer; following the selection of the first queue for each switch input accepting a nominating switch output in the first crossbar, setting each queue list pointer to a second queue, next in sequence to the first queue; and,

selecting a queue closest in succession to the second queue for each switch input accepting a nominating switch output in a second crossbar, and,

transferring information packets across the links, as recited in the claims.

The subject matter of claims 43, 54,56, and 58-61 is allowable over prior art of record, because all prior arts fail to teach or suggest an hierarchical arbitration system for transferring information across a switch, the system comprising:

a switch including a first plurality of crossbars having a plurality of parallel routed inputs and a plurality of parallel routed outputs connected to the switch inputs in response to the arbitration commands accepted on a control input;

an arbiter having an output connected to the switch control input to supply simultaneously arbitrated link commands for a plurality of links between the switch inputs and the switch outputs, for each crossbar;

a queue assembler having a plurality of inputs to accept variably sized information packets having a plurality of cells and addressing a plurality of outputs, and a control input to accept queue selection commands, the queue assembler grouping the information packets by switch output address, queuing the information packets into a plurality of queues for each address grouping, and supplying queues, selected in response to queue selection commands, at a plurality of outputs connected to corresponding switch inputs; and,

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wherein the switch locks the links between switch inputs and switch outputs, in response to commands from the arbiter, to transfer information packets across the links; and,

wherein the arbiter includes a crossbar counter to select a crossbar, and in response to a selected crossbar, simultaneously arbitrates between each arbitrating switch output and nominated switch inputs from an available switch in priority list, by selecting the least recently used available switch input in a plurality of arbitration cycles for each crossbar, as follows:

the arbiter nominates the highest priority available switch input for each arbitrating switch output, in first arbitration cycle, and if the nominating switch output is not accepted, the arbiter nominates successively lower priority available switch inputs in subsequent arbitration cycles;

each available switch input priority list includes a sequential input pointer that, following the acceptance of a list nominating switch output by a first switch input, is incremented to a second switch input, next in sequence to the first switch input; and,

the arbiter nominates the available switch input closest in succession to the second switch input in subsequent arbitrations;

wherein the arbiter arbitrates between the nominating switch outputs in response to a switch input receiving multiple switch output nominations by accepting the least recently available nominating switch output as follows:

the arbiter accepts nominating switch outputs in response to a nominating switch output priority lists, for each switch input receiving a plurality of nominating switch outputs;

each nominating switch output priority list includes a sequential output pointer that, following the acceptance of a nominating switch output, is incremented to a second switch output, next in sequence to the first switch output; and,

the arbiter accepts the nominating switch output closest in succession to second switch output in subsequent arbitrations, as recited in the claims

The subject matter of claims 62 and 65-71 is allowable over prior art of record, because all prior arts fail to teach or suggest a hierarchical arbitration system for transferring information across a switch, the system comprising:

a switch including a first plurality of crossbars having a plurality of parallel routed inputs and a plurality of parallel routed outputs connected to the switch inputs in response to the arbitration commands accepted on a control input;

an arbiter having an output connected to the switch control input to supply simultaneously arbitrated link commands for a plurality of links between the switch inputs and the switch outputs, for each crossbar;

a queue assembler having a plurality of inputs to accept variably sized information packets having a plurality of cells and addressing a plurality of outputs, and

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a control input to accept queue selection commands, the queue assembler grouping the information packets by switch output address, queuing the information packets into a plurality of queues for each address grouping, and supplying queues, selected in response to queue selection commands for each crossbar, at a plurality of outputs connected to corresponding switch inputs; and,

wherein the switch locks the links between switch inputs and switch outputs, in response to commands from the arbiter, to transfer information packets across the links;

wherein the arbiter includes a queue list with a queue pointer directed to a first queue, for each switch input, and selects the least recently available queue as follows:

in response to the queue pointer, the arbiter selects the first queue for each switch input accepting a nominating switch output for a first crossbar;

wherein the queue pointers, following the selection of each first queue, are incremented to a second queue, next in sequence to the first queue; and,

wherein the arbiter selects queues closest in succession to the second queue for each switch input accepting a nominating switch output for the second crossbar; and,

wherein the arbiter selects the least recently available queue for each crossbar, as recited in the claims.

The subject matter of claim 72 is allowable over prior art of record, because all prior arts fail to teach or suggest a hierarchical arbitration method in a switch system

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including a first-plurality of crossbars with a plurality of parallel routed switch inputs and a plurality of parallel routed switch outputs, comprising:

accepting variably sized information packets having a ranked class of service (COS) and including a plurality of cells at a plurality of switch inputs, the plurality of information packets addressing a plurality of switch outputs;

at each switch input, queuing the information packets by COS into a plurality of queues;

simultaneously arbitrating for a plurality links between switch inputs and switch outputs;

locking the links:

establishing a plurality of selection cycles;

simultaneously analyzing information packets at the head of each queue in each selection cycle;

selecting a queue for each locked link, for each crossbar, wherein each nominated switch input selecting a queue in response to COS of the information packets available for each crossbar; and,

transferring information packets across the links, as recited in the claim.

The subject matter of claim 73 is allowable over prior art of record, because all prior arts fail to teach or suggest a hierarchical arbitration system for transferring information across a switch, the system comprising:

a switch including a first plurality of crossbars having a plurality of parallel routed inputs and a plurality of parallel routed outputs connected to the switch inputs in response to the arbitration commands accepted on a control input;

an arbiter having an output connected to the switch control input to supply simultaneously arbitrated link commands for a plurality of links between the switch inputs and the switch outputs, for each crossbar;

a queue assembler having a plurality of inputs to accept variably sized information packets having a ranked class of service (COS) with a plurality of cells and addressing a plurality of outputs, and a control input to accept queue selection commands, the queue assembler grouping the information packets by switch output address, queuing the information packets into a plurality of queues for each address grouping by COS, and supplying queues, selected in response to queue selection commands for each crossbar, at a plurality of outputs connected to corresponding switch inputs;

wherein the switch locks the links between switch inputs and switch outputs, in response to commands from the arbiter, to transfer information packets across the links:

wherein the arbiter selects a queue in response to COS of the information packet available for each crossbar, by establishing a plurality of selection cycles

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per minor decision cycle, and simultaneously analyzes information packet, as recited in the claim.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

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Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lina Yang whose telephone number is (571)272-3151. The examiner can normally be reached Monday through Wednesday between 7:00 a.m. and 7:30 p.m. eastern standard time.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Vu can be reached on (571) 272-3155. The fax phone number for the organization where this application or proceeding is assigned is 517-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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ALPUS H. HSU PRIMARY EXAMINER

Alpm vs. 200